WHAT IS CLAIMED IS:

1.   A data shuffler apparatus for shuffling input bits comprising:

a plurality of bit shufflers each inputting corresponding two bits x_0 and x_1 of the input bits and outputting a 2-bit vector $\{x_0', x_1'\}$;

two 2-bit vector shufflers inputting the 2-bit vectors $\{x0', x1'\}$, wherein an output of the 2-bit vector shufflers is a combination of corresponding two 2-bit vectors $\{x0', x1'\}$, such that the 2-bit vector shufflers operate on the 2-bit vectors $\{x0', x1'\}$ in the same manner as the bit shufflers operate on the bits $x0$ and $x1$,

wherein the current state of the bit shufflers is updated based on a previous state of the 2-bit vector shufflers.

2.   The apparatus of claim 1, wherein, in the vector $\{x_0', x_1'\}$, a number of 1's at bit x_0' over time is within +/-1 of a number of 1's at bit x_1'.

3.   The apparatus of claim 2, wherein the vector $\{x_0', x_1'\}$ is defined by:

Current State of Bit Shuffler	Input Bits	Next State of Bit Shuffler	Vector $\{x_0', x_1'\}$
S_0 (0)	$x_0 = x_1$	S_0 (0)	$\{x_0, x_1\}$
S_0 (0)	$x_0 \neq x_1$	S_1 (1)	$\{x_1, x_0\}$
S_1 (1)	$x_0 = x_1$	S_1 (1)	$\{x_0, x_1\}$
S_1 (1)	$x_0 \neq x_1$	S_0 (0)	$\{x_0, x_1\}$

4.   The apparatus of claim 1, wherein the 2-bit vector shuffler output 4-bit vectors.

5.   The apparatus of claim 1, further comprising at least one 4-bit vector shuffler taking as an input two 4-bit vectors produced by two 4-bit vector shufflers, and outputting an 8-bit vector,

wherein the 4-bit vector shuffler operates on the two 4-bit vectors in the same manner as each bit shuffler operates on the bits x_0 and x_1, and

wherein the current state of the bit shufflers is updated based on a previous state of the 4-bit vector shuffler.

6.   The apparatus of claim 4, further comprising at least one 4-bit vector shuffler inputting two 4-bit vectors produced by the two 2-bit vector shufflers, and outputting an 8-bit vector,

wherein the 4-bit vector shuffler operates on the 4-bit vectors in the same manner as each bit shuffler operates on the bits x_0 and x_1, and

wherein the current state of the bit shufflers is updated based on a previous state of the 4-bit vector shuffler.

7.   A digital to analog converter comprising:

an interpolation filter receiving an N-bit digital input;

a delta-sigma modulator receiving an output of the interpolation filter; and

a dynamic element matching encoder receiving N bits from the delta-sigma modulator, and outputting an analog signal corresponding to the digital input,

wherein the dynamic element matching encoder includes:

a plurality of bit shufflers each inputting two bits x_0 and x_1 of the N bits, and outputting a vector $\{x_0', x_1'\}$; and

a plurality of vector shufflers arranged both in parallel and in successive levels, inputting the vectors $\{x_0', x_1'\}$ and outputting vectors each corresponding to a combination of vectors produced by a previous set of shufflers,

wherein the vector shufflers operate on their respective input vectors in the same manner as the bit shufflers operate on the bits x_0 and x_1, and

wherein the current state of the bit shufflers is updated based on a previous state of the last level of the vector shufflers.

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8. The digital to analog converter converter of claim 7, further comprising a low pass filter for filtering the analog signal.

9. The digital to analog converter of claim 7, wherein, in the vector $\{x_0', x_1'\}$, a number of 1's at bit x_0' over time is within +/-1 of a number of 1's at bit x_1'.

10. The digital to analog converter of claim 7, wherein the 2-bit vector shuffler output 4-bit vectors.

11. The digital to analog converter of claim 7, wherein the vector $\{x_0', x_1'\}$ is defined by:

Current State of Bit Shuffler	Input Bits	Next State of Bit Shuffler	Vector $\{x_0', x_1'\}$
S_0 (0)	$x_0 = x_1$	S_0 (0)	$\{x_0, x_1\}$
S_0 (0)	$x_0 \neq x_1$	S_1 (1)	$\{x_1, x_0\}$
S_1 (1)	$x_0 = x_1$	S_1 (1)	$\{x_0, x_1\}$
S_1 (1)	$x_0 \neq x_1$	S_0 (0)	$\{x_0, x_1\}$

12. The digital to analog converter of claim 7, further comprising at least one 4-bit vector shuffler taking as an input two 4-bit vectors produced by two 4-bit vector shufflers, and outputting an 8-bit vector,

wherein the 4-bit vector shuffler operates on the two 4-bit vectors in the same manner as each bit shuffler operates on the bits x_0 and x_1, and

wherein the current state of the bit shufflers is updated based on a previous state of the 4-bit vector shuffler.

13. A digital to analog converter comprising:

an interpolation filter receiving an N-bit digital input;

a delta-sigma modulator receiving an output of the interpolation filter; and

a dynamic element matching encoder receiving N bits from the delta-sigma modulator, and outputting an analog signal corresponding to the digital input,

wherein the dynamic element matching encoder includes:

a plurality of bit shufflers each inputting corresponding two bits x_0 and x_1 of the input bits and outputting a 2-bit vector $\{x_0', x_1'\}$;

two 2-bit vector shufflers inputting the 2-bit vectors $\{x_0', x_1'\}$, wherein an output of the 2-bit vector shufflers is a combination of corresponding two 2-bit vectors $\{x_0', x_1'\}$, such that the 2-bit vector shufflers operate on the 2-bit vectors $\{x_0', x_1'\}$ in the same manner as the bit shufflers operate on the bits x_0 and x_1,

wherein the current state of the bit shufflers is updated based on a previous state of the 2-bit vector shufflers.

14.   The digital to analog converter of claim 13, further comprising a low pass filter for filtering the analog signal.

15.   The digital to analog converter of claim 13, wherein, in the vector $\{x_0', x_1'\}$, a number of 1's at bit x_0' over time is within +/-1 of a number of 1's at bit x_1'.

16.   The digital to analog converter of claim 13, wherein the 2-bit vector shuffler output 4-bit vectors.

17.   The digital to analog converter of claim 13, wherein the vector $\{x_0', x_1'\}$ is defined by:

Current State of Bit Shuffler	Input Bits	Next State of Bit Shuffler	Vector $\{x_0', x_1'\}$
S_0 (0)	$x_0 = x_1$	S_0 (0)	$\{x_0, x_1\}$
S_0 (0)	$x_0 \neq x_1$	S_1 (1)	$\{x_1, x_0\}$
S_1 (1)	$x_0 = x_1$	S_1 (1)	$\{x_0, x_1\}$
S_1 (1)	$x_0 \neq x_1$	S_0 (0)	$\{x_0, x_1\}$

18.   The digital to analog converter of claim 13, further comprising at least one 4-bit vector shuffler taking as an input two 4-bit vectors produced by two 4-bit vector shufflers, and outputting an 8-bit vector,

wherein the 4-bit vector shuffler operates on the two 4-bit vectors in the same manner as each bit shuffler operates on the bits x_0 and x_1, and

wherein the current state of the bit shufflers is updated based on a previous state of the 4-bit vector shuffler.

19.   A method of shuffling a plurality of input bits comprising:

shuffling each set of two bits x_0 and x_1 of the input bits into corresponding vectors $\{x_0', x_1'\}$;

shuffling the 2-bit vectors $\{x_0', x_1'\}$ into 4-bit vectors each corresponding to a shuffled combination of two 2-bit vectors $\{x_0', x_1'\}$, such that the 4-bit vectors are shuffled in the same manner as the bits x_0 and x_1 are shuffled; and

updating a current state based on a previous state resulting from shuffling the 4-bit vectors.

20.   The method of claim 18, wherein, in the vector $\{x_0', x_1'\}$, a number of 1's at bit x_0' over time is within +/-1 of a number of 1's at bit x_1'.

21.   The method of claim 18, wherein the vector $\{x_0', x_1'\}$ is defined by:

Current State of Bit Shuffler	Input Bits	Next State of Bit Shuffler	Vector $\{x_0', x_1'\}$
S_0 (0)	$x_0 = x_1$	S_0 (0)	$\{x_0, x_1\}$
S_0 (0)	$x_0 \neq x_1$	S_1 (1)	$\{x_1, x_0\}$
S_1 (1)	$x_0 = x_1$	S_1 (1)	$\{x_0, x_1\}$
S_1 (1)	$x_0 \neq x_1$	S_0 (0)	$\{x_0, x_1\}$

22.   The method of claim 18, further comprising the steps of:

inputting the 4-bit vectors, and outputting an 8-bit vector, wherein the 4-bit vectors are shuffled in the same manner as the bit inputs x_0 and x_1; and

updating the current state used for shuffling the bits x_0 and x_1 based on a previous state resulting from shuffling the 4-bit vectors.

23.   A method of converting a digital signal to an analog signal comprising:

filtering the digital signal with an interpolation filter;

modulating an output of the interpolation filter with a delta-sigma modulator to produce an N bit signal;

receiving the N bits from the delta-sigma modulator;

shuffling each set of bits x_0 and x_1 of the N bits and outputting a vector $\{x_0', x_1'\}$;

shuffling the vectors $\{x_0', x_1'\}$ into 2-bit vectors in the same manner as the bits x_0 and x_1 are shuffled;

updating a current state of the bits x_0 and x_1 based on a previous state used for shuffling the 2-bit vectors; and

outputting an analog signal corresponding to the digital signal, wherein the input bits are maximally balanced with respect to the centerlines of all the input bits, each half of the input bits, and each quarter of the input bits.

24.   The method of claim 22, wherein, in the vector $\{x_0', x_1'\}$, a number of 1's at bit x_0' over time is within +/-1 of a number of 1's at bit x_1'.

25.   The method of claim 22, wherein the vector $\{x_0', x_1'\}$ is defined by:

Current State of Bit Shuffler	Input Bits	Next State of Bit Shuffler	Vector $\{x_0', x_1'\}$
S_0 (0)	$x_0 = x_1$	S_0 (0)	$\{x_0, x_1\}$
S_0 (0)	$x_0 \neq x_1$	S_1 (1)	$\{x_1, x_0\}$
S_1 (1)	$x_0 = x_1$	S_1 (1)	$\{x_0, x_1\}$
S_1 (1)	$x_0 \neq x_1$	S_0 (0)	$\{x_0, x_1\}$